

17439 U.S. PTO
121603

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor Patent Application of: Wendell P. Noble Jr.

Title: **VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME**

Attorney Docket No.: 303.412US4

Customer No.: 21186

PATENT APPLICATION TRANSMITTAL

MAIL STOP PATENT APPLICATION

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

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We are transmitting herewith the following attached items and information (as indicated with an "X"):

- ☒ Return postcard.
- ☒ **DIVISIONAL** of prior Patent Application No.(09/879602) (under 37 CFR 1.53(b)) comprising:
 - ☒ Specification (26 pgs, including claims numbered 1 through 25 and a 1 page Abstract).
 - ☒ Formal Drawing(s) (10 sheets).
 - ☒ Copy of signed Declaration (3 pgs)from prior application.
 - ☒ Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
 - ☒ Check in the amount of \$1032.00 to pay the filing fee.
- ☒ Prior application is assigned of record to Micron Technology, Inc..
- ☒ Information Disclosure Statement (1 pgs), Form 1449 (8 pgs) References NOT enclosed, cited in prior application.
- ☒ Communication Concerning Related Applications (6 pgs.).

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	25-20	5	x 18.00 =	\$90.00
INDEPENDENT CLAIMS	5-3	2	x 86.00 =	\$172.00
[] MULTIPLE DEPENDENT CLAIMS PRESENTED				\$0.00
BASIC FEE				\$770.00
TOTAL				\$1032.00

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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S/N Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble Jr. Examiner: Unknown
Serial No.: Unknown Group Art Unit: Unknown
Filed: Herewith Docket: 303.412US4
Title: VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM
ACCESS MEMORY AND METHOD FOR FORMING THE SAME

COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
08/889463 6072209	July 8, 1997	303.322US1	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
09/527981	March 17, 2000	303.322US2	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
09/571352 6476434	May 16, 2000	303.322US3	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
08/889395 6191470	July 8, 1997	303.323US1	SEMICONDUCTOR-ON-INSULATOR MEMORY CELL WITH BURIED WORD AND BODY LINES
09/510095 6465298	February 22, 2000	303.323US2	SEMICONDUCTOR-ON-INSULATOR MEMORY CELL WITH BURIED WORD AND BODY LINES
08/889462 6150687	July 8, 1997	303.328US1	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: Unknown

Filing Date: Herewith

Title: VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME

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09/139164 6350635	August 24, 1998	303.328US2	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
09/596266 6399979	June 16, 2000	303.328US3	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
09/651199 6504201	August 30, 2000	303.328US4	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
08/889396 5909618	July 8, 1997	303.329US1	METHOD OF MAKING MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES
09/031620 6104061	February 27, 1998	303.329US2	MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES
09/520649 6191448	March 7, 2000	303.329US3	MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES
09/789274 6492233	February 20, 2001	303.329US4	MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES
08/889554 5973356	July 8, 1997	303.330US1	ULTRA HIGH DENSITY FLASH MEMORY
09/035304 6238976	February 27, 1998	303.330US2	A METHOD FOR FORMING HIGH DENSITY FLASH MEMORY
09/866938	May 29, 2001	303.330US3	ULTRA HIGH DENSITY FLASH MEMORY

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: Unknown

Filing Date: Herewith

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08/889553 5936274	July 8, 1997	303.342US1	HIGH DENSITY FLASH MEMORY
09/137328 6143636	August 20, 1998	303.342US2	HIGH DENSITY FLASH MEMORY
08/939742 6066869	October 6, 1997	303.379US1	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
09/551027	April 17, 2000	303.379US2	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
08/944890 6528837	October 6, 1997	303.380US1	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/143606 6156604	August 31, 1998	303.380US2	METHOD FOR MAKING AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/730245 6610566	December 5, 2000	303.380US3	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/010729 6025225	January 22, 1998	303.389US1	CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO- ROUGHENED SEMICONDUCTOR SURFACES AND METHODS FOR FORMING THE SAME
09/467992	December 20, 1999	303.389US2	CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO- ROUGHENED SEMICONDUCTOR SURFACES

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: Unknown

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Title: VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME

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08/944312 5914511	October 6, 1997	303.391US1	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY USING TRENCH PLATE CAPACITOR CELLS WITH BODY BIAS CONTACTS
09/138796 6156607	August 24, 1998	303.391US2	METHOD FOR A FOLDED BIT LINE MEMORY USING TRENCH PLATE CAPACITOR CELLS WITH BODY BIAS CONTACTS
08/939732 5907170	October 6, 1997	303.393US1	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/138794 6165836	August 24, 1998	303.393US2	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/742568 6537871	December 20, 2000	303.393US3	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/028249 5963469	February 24, 1998	303.399US1	VERTICAL BIPOLAR READ ACCESS FOR LOW VOLTAGE MEMORY CELL
09/328074 6317357	June 8, 1999	303.399US2	VERTICAL BIPOLAR READ ACCESS FOR LOW VOLTAGE MEMORY CELL
09/031621 5991225	February 27, 1998	303.405US1	PROGRAMMABLE MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS
09/313049 6153468	May 17, 1999	303.405US2	PROGRAMMABLE MEMORY ADDRESS DECODE ARRAYS WITH VERTICAL TRANSISTOR
09/669281	September	303.405US3	PROGRAMMABLE MEMORY

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: Unknown

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Title: VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME

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6597037	26, 2000		ADDRESS DECODE ARRAYS WITH VERTICAL TRANSISTOR
09/032617 6124729	February 27, 1998	303.406US1	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS
09/520494 6486027	March 8, 2000	303.406US2	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS
09/129047 6208164	August 4, 1998	303.407US1	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/756089 6515510	January 8, 2001	303.407US2	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/756099 6486703	January 8, 2001	303.407US3	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/128848 6134175	August 4, 1998	303.408US1	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS
09/650600 6498065	August 30, 2000	303.408US2	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS
09/028805 6242775	February 24, 1998	303.410US1	CIRCUITS AND METHODS USING VERTICAL, COMPLEMENTARY TRANSISTORS
09/514493 6294418	February 29, 2000	303.410US2	CIRCUITS AND METHODS USING VERTICAL, COMPLEMENTARY TRANSISTORS
09/028807 6246083	February 24, 1998	303.412US1	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME

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Serial Number: Unknown

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Title: VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME

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09/879592	June 12, 2001	303.412US2	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME
09/028727 6304483	February 24, 1998	303.462US1	CIRCUITS AND METHODS FOR A STATIC RANDOM ACCESS MEMORY USING VERTICAL TRANSISTORS
09/060048 6043527	April 14, 1998	303.464US1	CIRCUITS AND METHODS FOR A MEMORY CELL WITH A TRENCH PLATE TRENCH CAPACITOR AND A VERTICAL BIPOLAR READ DEVICE
09/498433 6381168	February 4, 2000	303.464US2	CIRCUITS AND METHODS FOR A MEMORY CELL WITH A TRENCH PLATE TRENCH CAPACITOR AND A VERTICAL BIPOLAR READ DEVICE
10/361986	February 11, 2003	303.380US4	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR

Respectfully submitted,

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